

REMARKS

Applicants respectfully request reconsideration of this application in view of the foregoing amendments and the following remarks.

Claim Status

Claims 1-27 are pending in this application. Claims 1-9, 12-17, 21-23, 26 and 27 have been rejected. Claims 10, 11, 18, 19, 24 and 25 have been objected to by the Examiner. Claims 1 and 14 are herein amended. No new matter has been added by these amendments.

Rejections Under 35 U.S.C. § 102

Claims 14-17 have been rejected under 35 U.S.C. § 102(a) as being anticipated by Applicants' admitted prior art (APA).

With regard to independent claim 14, the Examiner asserted that APA teaches all the claimed elements. Applicants respectfully disagree.

Claim 14 of the present invention recites,

A delay locked loop (DLL), comprising;
a basic clock generator for generating a plurality of basic clock signals which are each shifted in response to an external signal;
a first mixer for generating a first clock signal in response to the plurality of basic clock signals;
a second mixer for generating a second clock signal which is 90 degrees out-of-phase with the first clock signal in response to the plurality of basic clock signals;
a clock buffer for generating a first internal clock signal in response to the first clock signal and a second internal clock signal in response to the second clock signal and in consideration of a line load of the first internal clock signal;
a phase detector for comparing and detecting phases of the external clock signal and the second internal clock signal; and

a digital-to-analog converter for controlling phase ranges of the first and second clock signals generated in first and second mixers in response to an output of the phase detector.

In contrast to the present invention as recited in claim 14, APA does not disclose at least “a second mixer for generating a second clock signal which is 90 degrees out-of-phase with the first clock signal in response to the plurality of basic clock signals”. Instead, APA discloses only one mixer 104 for generating a second clock signal by mixing two basic clock signals selected in response to the output of a digital-to-analog converter. There is no disclosure in APA of two mixers only one mixer. Moreover, element 105a, which was also indicated by the Examiner as being the “second mixer”, is a delay device not a mixer. Thus, because there is no disclosure in APA of two mixers and in particular a “second mixer” as recited in claim 14, Applicants believe the invention as recited therein is patentable over APA.

Rejections Under 35 U.S.C. § 103

Claims 1-9, 12, 20-23 and 26 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over APA in view of U.S. Patent No. 5,764,091 (Sumita).

With regard to independent claim 5, the Examiner asserted that APA shows all the elements claimed therein except for a “second duty corrector [210’ of FIG. 2] for correcting the duty of [an] internal clock signal ...” However, the Examiner further asserted that Sumita discloses “a semiconductor integrated circuit having a duty corrector circuit (10) for each of the plurality of internal clocks wherein each of the internal clocks [is] associated with a circuit block (51a-51d)”. Thus, according to the Examiner, it would have been obvious to one of ordinary skill in the art to “utilize [the] teaching of Sumita ... by implementing a duty corrector ... for correcting a duty of the first internal clock

signal for the advantage of being able to provide a duty-ratio guaranteed of the first internal clock signal". Applicants respectfully disagree.

As correctly pointed out by the Examiner, APA does not disclose "a second duty corrector [210' of FIG. 2] for correcting the duty of [an] internal clock signal ..." as recited in claim 5 of the present invention. Instead, APA discloses a DLL that includes, *inter alia*, a first duty corrector for compensating for the duty of a first clock signal generated by a first amplifier and a second duty corrector for correcting duty errors in a first internal clock signal.

With regard to Sumita, Sumita is directed to a method and system for correcting the duty ratio of a circuit-drive clock signal on the basis of a reference clock signal. In particular, Sumita discloses a semiconductor integrated circuit including circuit blocks that are fed a drive clock signal generated by a clock generator. A clock signal waveform correction system (CSWS) is found in one of the circuit blocks. In operation, the CSWS receives the drive clock signal and a duty ratio-guaranteed reference clock signal for correcting the duty of the drive clock signal.

Sumita does not, however, disclose a "second duty corrector for correcting the duty of [a] first internal clock signal and feeding an output of the second duty corrector back to [a] second amplifier ..." as recited in claim 5. To the contrary, Sumita discloses a single CSWS that corrects the duty of a drive clock signal using a duty ratio-guaranteed reference clock signal. In addition, Sumita does not disclose feeding the corrected drive clock signal to a second amplifier as recited in claim 5. Thus, one of ordinary skill in the art would not look to the CSWS of Sumita, especially since it is not compatible with the duty controllers of APA as it requires a duty ratio-guaranteed reference clock signal for

duty correction, and combine it with APA to make the present invention recited in claim 5. As such, Applicants believe that the invention as recited in claim 5 is patentable over the cited art of record because neither APA taken alone or in combination with Sumita, teaches, discloses or suggests the invention as recited therein.

Claims 1 and 20 were rejected for essentially the same reasons as claim 5. Accordingly, claims 1 and 20 are believed to be allowable for at least the same reasons as discussed above with reference to claim 5.

Claims 13 and 27 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over APA in view of Sumita and further in view of U.S. Patent No. 5,911,063 (Allen). Claims 13 and 27 are believed to be allowable for at least the reasons discussed above with respect to independent claims 5 and 20 from which they depend.

Claims 1 and 14 were amended to remedy grammatical deficiencies therein.

Claim Objections

Claims 10, 11, 18, 19, 24 and 25 have been objected to as being dependent upon a rejected base claim, but would allowable if rewritten in dependent form including all the limitations of their base claims and any intervening claims. The remarks above with respect to claims 1, 5, 14 and 20 from which claims 10, 11, 18, 19, 24 and 25 depend render moot the objections to these claims.

Dependent Claims

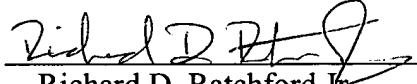
Applicants have not independently addressed the rejections of all the dependent claims because Applicants submit that, in view of the amendments to the claims presented herein and, for at least similar reasons as why the independent claims from which the dependent claims depend are believed allowable as discussed, *supra*, the

dependent claims are also allowable. Applicants however, reserve the right to address any individual rejections of the dependent claims should such be necessary or appropriate.

CONCLUSION

Accordingly, Applicants submit that the claims as herein presented are allowable over the prior art of record, taken alone or in combination, and that the respective rejections be withdrawn. Applicants further submit that the application is hereby placed in condition for allowance which action is earnestly solicited.

Respectfully submitted,

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